

1 kV, 10-kW SiC-Based Quadruple Active Bridge DCX Stage in a DC to Three-Phase AC Module for Medium-Voltage Grid Integration

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Abstract—Interfacing low voltage dc to medium voltage three-phase ac grid is often based on series-stackable modular converter architectures. To minimize energy storage requirements, it is advantageous to employ a quadruple active bridge (QAB) stage operating as a “dc transformer” in each stackable module. The QAB stage offers three isolated dc link voltages, which then allow for flexible stacking of three single-phase dc-to-ac inverter stages. Each of the module phases processes a pulsating power having a component at twice the line frequency. This presents a challenge in maintaining zero voltage switching (ZVS) on the secondary sides of the QAB during low-power portions of the line cycle. This article is focused on the design of the QAB stage. A detailed analysis of ZVS switching waveforms is presented, including effects of nonlinear device capacitances. It is shown how ZVS can be achieved at all times using a relatively small circulating current provided by the magnetizing inductance of the high-frequency transformer. Analytical expressions are given for the optimal values of the magnetizing inductance and the dead times of the QAB primary and secondary bridges. The approach is verified by experimental results on a 1 kV, 10-kW SiC-based prototype, demonstrating a relatively flat efficiency curve with a peak efficiency of 97.1% at 75% load.

Index Terms—Dual active bridge, medium voltage (MV) ac, modular dc-to-ac inverters, photovoltaic power systems, quadruple active bridge (QAB), solid-state transformers (SSTs), zero voltage switching (ZVS).

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I. INTRODUCTION

MODULAR power electronics architectures have gained increased attention as interfaces between low voltage (LV) dc or ac systems and the medium voltage (MV) ac grid, replacing bulky line frequency transformers [1]. Modular solid-state transformers (SST) and similar architectures have been used in electric vehicle (EV) dc charges [2]–[5], power distribution for data centers [6], photovoltaic (PV) power systems [7]–[9], and other applications.

Fig. 1 shows a stackable modular architecture, where each module has a dc port and three isolated single-phase ac ports [9]. The module dc port and the ac ports can be used independently, or stacked in parallel or in series. For example, in the architecture shown in Fig. 1, the dc ports are tied to LV dc sources, such as PV strings, while ac ports stacked in series are connected to an MV three-phase grid. The architecture features an interesting property of eliminating twice the line frequency pulsating power on the dc port of each module, thus eliminating the need for bulky energy storage. As shown in Fig. 2, each module contains a quadruple active bridge (QAB) creating three isolated dc link voltages, each followed by a single-phase dc–ac inverter bridge. The QAB, which operates as a fixed-ratio converter, i.e., as “dc transformer” (DCX), provides galvanic isolation between the primary and each of the individual ac phases, so the modules can be flexibly stacked on the ac side.

The QAB outputs connected to phases *A*, *B*, and *C* deliver time-varying power $p_A(t)$, $p_B(t)$, and $p_C(t)$, respectively, each having a dc and twice-line-frequency ac component. The three currents add up on the primary side, such that dc power is transferred from the input, and the dc-link capacitance requirements are relaxed. This is an advantage compared to single-phase systems where the dc-link capacitors are sized for energy storage at twice the line frequency [10], [11]. In contrast, the dc-link capacitors are sized here to filter the switching ripple in the secondary-bridge output current and the inverter input current.

The fact that the power fluctuates from zero to twice the average power on each secondary side during a line cycle presents challenges with respect to soft-switching of the secondary side bridges. This is similar to the loss of zero-voltage switching

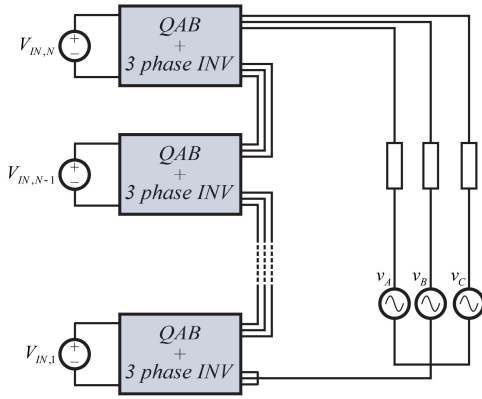


Fig. 1. System architecture with cascaded isolated inverter modules [9]. The module configuration is shown in Fig. 2.

(ZVS) in lightly loaded dual-active-bridge (DAB) dc–dc converters, where inductively stored energy is insufficient to achieve soft charging and discharging of the switching-node capacitance [12], [13]. This capacitance consists of power MOSFET capacitances, inductor and transformer winding capacitance, and printed circuit board (PCB) parasitic capacitance.

DAB converters have been used in applications that process ac power, such as ac–dc rectifiers [14]–[16] and ac–ac converters [17]. A modulation strategy for operating DABs under soft switching conditions throughout the entire operating range was proposed in [18], but the effects of the device output capacitances were not fully taken into account. Kheraluwala *et al.* [12] showed that a reduced magnetizing inductance can lead to an extended ZVS range, but interactions between the magnetizing inductance and the device output capacitances were not addressed. Utilization of the transformer magnetizing current to extend ZVS to light load region was also proposed in [19] and [20]. This approach relies on relatively complex high-resolution dead-time control to account for multiple resonant periods, which in practice may result in the loss of ZVS. Facilitating ZVS transitions by utilizing magnetizing current was also discussed in [21] for a DCX based on a series resonant converter (SRC).

Switching transitions and ZVS conditions in the QAB stage shown in Fig. 2 differ from the conditions in DAB converters, so that aforementioned previously reported analysis and mitigation techniques do not directly apply. Unique to the QAB stage in Fig. 2 is that, assuming a balanced three-phase system, the primary-side power is dc, which means that ZVS can be accomplished throughout the line cycle on the primary bridge. However, the loss of ZVS on the secondary side during low-power intervals of an ac line period results in reduced system efficiency. This article proposes a solution for ZVS operation of the QAB over the entire ac line cycle by optimally utilizing the magnetizing currents of the transformers (or separate auxiliary inductors), as illustrated in Fig. 2 [22]. By reducing the magnetizing inductance of the transformer, circulating currents are introduced through the secondary sides of the QAB. The circulating currents greatly reduce switching loss at the cost of slightly increased conduction loss.

The reduced magnetizing inductance is not needed to achieve ZVS at all points during the line cycle at full load. However, while operating at lower average power levels, the energy provided by the series inductance becomes insufficient to achieve ZVS over a larger portion of the line cycle, which is why the circulating current due to the reduced magnetizing inductance helps with ZVS and results in improved efficiency. As an alternative, a larger series inductance could be used, but this approach would result in reduced efficiency at full load.

A detailed analysis of the switching sequence during primary and secondary dead-time intervals and the ZVS transition at zero power transfer is given in Section II. A design procedure is developed in Section III to select the converter parameters to minimize the circulating currents, while maintaining ZVS at all times. The critical zero-power operating point is discussed in detail, including parasitic capacitance effects, and approximate closed form expressions are found for choosing the magnetizing inductance and the dead times. The nonlinear nature of the device parasitic capacitance is taken into account based on the approach described in [23]. Section IV investigates how the choice of the maximum phase shift, for a given power level, affects losses in the converter, assuming the design discussed in Section II. The loss analysis addresses major loss mechanisms, including semiconductor conduction losses, as well as core and conduction losses in the magnetics. The optimal values of the maximum phase shift and, thereby the series inductance are chosen to minimize the losses. Experimental verification results on a 1 kV, 10-kW SiC-based prototype are presented in Section V. Finally, Section VI concludes this article.

II. ZERO VOLTAGE SWITCHING AT ZERO INSTANTANEOUS POWER TRANSFER IN ONE PHASE

To guarantee ZVS operation of a particular phase over the entire line cycle, it is sufficient to show how ZVS can be achieved at the zero power transfer instant. The solution presented in this section is based on sizing the magnetizing inductance and a proper combination of the primary and secondary-side dead times.

Over a line cycle, the power processed by each secondary is determined by the corresponding phase shift between the secondary and the primary full bridge

$$\begin{aligned}\varphi_A(t) &= \varphi_m \sin^2(\omega_0 t) \\ \varphi_B(t) &= \varphi_m \sin^2\left(\omega_0 t + \frac{2\pi}{3}\right) \\ \varphi_C(t) &= \varphi_m \sin^2\left(\omega_0 t - \frac{2\pi}{3}\right)\end{aligned}\quad (1)$$

where φ_m is the maximum phase shift, and ω_0 is the angular line frequency.

Consider the time instant when the power processed by phase A is zero, while phases B and C contribute nonzero instantaneous power levels to maintain constant overall power in the three-phase module. The corresponding switch control signals are shown in Fig. 3. The phase shift φ_A between the primary bridge and the phase A secondary bridge is zero, so that the

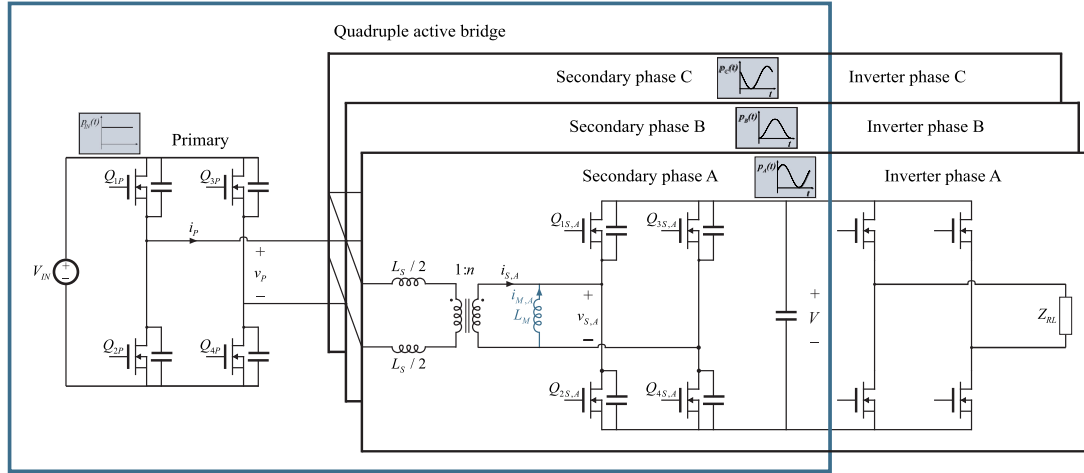


Fig. 2. Transformer-isolated inverter module using a quadruple active bridge (QAB) dc-dc converter operated as a fixed-ratio “dc transformer” (DCX).

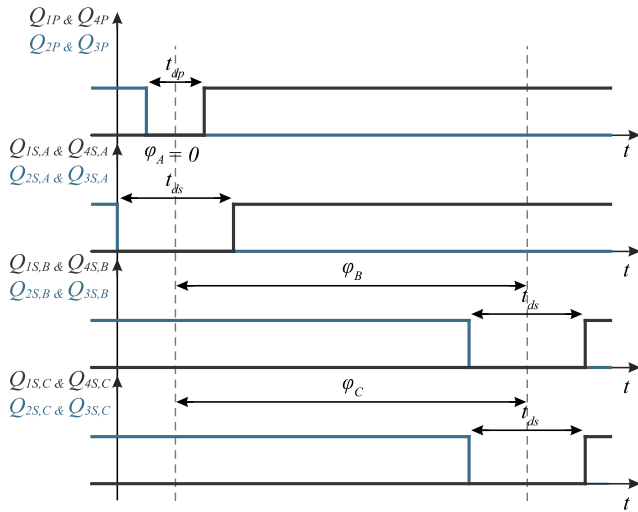


Fig. 3. QAB switch control signals at the time when the secondary Phase A processes zero power.

TABLE I
TIME INSTANTS OF THE SWITCHING SEQUENCE
DURING ZVS TRANSITION

T_1	$0.5(t_{ds} - t_{dp})$
T_2	$0.5(t_{ds} + t_{dp})$
T_3	t_{ds}

TABLE II
TIME INTERVALS OF THE SWITCHING SEQUENCE
DURING ZVS TRANSITION

Interval I	$0 \leq t < T_1$
Interval II	$T_1 \leq t < T_2$
Interval III	$T_2 \leq t < T_3$

corresponding control pulses are centered around the same instant. Theoretical, model-based waveforms during the rise-time transition of the secondary switching node are shown in Fig. 4. Definitions of the time instants and the time intervals during the transition are given in Tables I and II, while the corresponding

equivalent circuit models for the switching sequence consisting of Intervals I, II, and III are shown in Fig. 5.

At the beginning of time Interval I [Fig. 5(a)], the secondary side switches $Q_{2S,A}$ and $Q_{3S,A}$ are turned OFF. The magnetizing inductance current $i_{M,A}$ starts charging voltage-dependent switching-node capacitance $C_S(v)$ of the phase A secondary bridge, and the switching node voltage $v_{S,A}$ starts increasing. As $v_{S,A}$ increases, a negative voltage is applied across the series inductance, and the current $i_{S,A}$ starts decreasing.

The primary-side switches Q_{2P} and Q_{3P} turn OFF at the beginning of Interval II. The equivalent circuit in Interval II is shown in Fig. 5(b). During this interval, phases B and C are charging the switching-node capacitance $C_P(v)$ on the primary side. It is assumed that the QAB is closed-loop controlled to operate as a DCX, so that $v_{S,B}$ and $v_{S,C}$ can be considered constant voltage sources. The rise time of the primary side switching node v_P is faster than $v_{S,A}$, because the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much higher than the peak of the magnetizing current. This implies that $\frac{dv}{dt}$ across the series inductance parasitic capacitance C_{LS} is approximately constant, therefore, the constant current through C_{LS} charges $v_{S,A}$ linearly.

At the mid-point of Interval II, nv_P becomes higher than $v_{S,A}$, and the slope of $i_{S,A}$ changes polarity. Interval II ends, completing the ZVS transition of v_P , at the end of the primary-side dead time t_{dp} .

Interval III starts with turning ON switches Q_{1P} and Q_{4P} of the primary full bridge. The corresponding equivalent circuit is shown in Fig. 5(c). During this interval, current $i_{S,A}$ is increasing until $v_{S,A}$ reaches the end of the ZVS transition. At that instant, $Q_{1S,A}$ and $Q_{4S,A}$ are turned ON, which ends Interval III and the secondary phase A dead time t_{ds} .

It should be noted that the total current that charges the switching node capacitance

$$i_{\text{tot},A} = i_{S,A} + i_{M,A} + i_{C_{LS},A} \quad (2)$$

reaches a minimum at the beginning of the Interval II. If this current became negative, it would start discharging the secondary side switching-node capacitance $C_S(v)$, which means that it would not be possible to complete the ZVS switching sequence

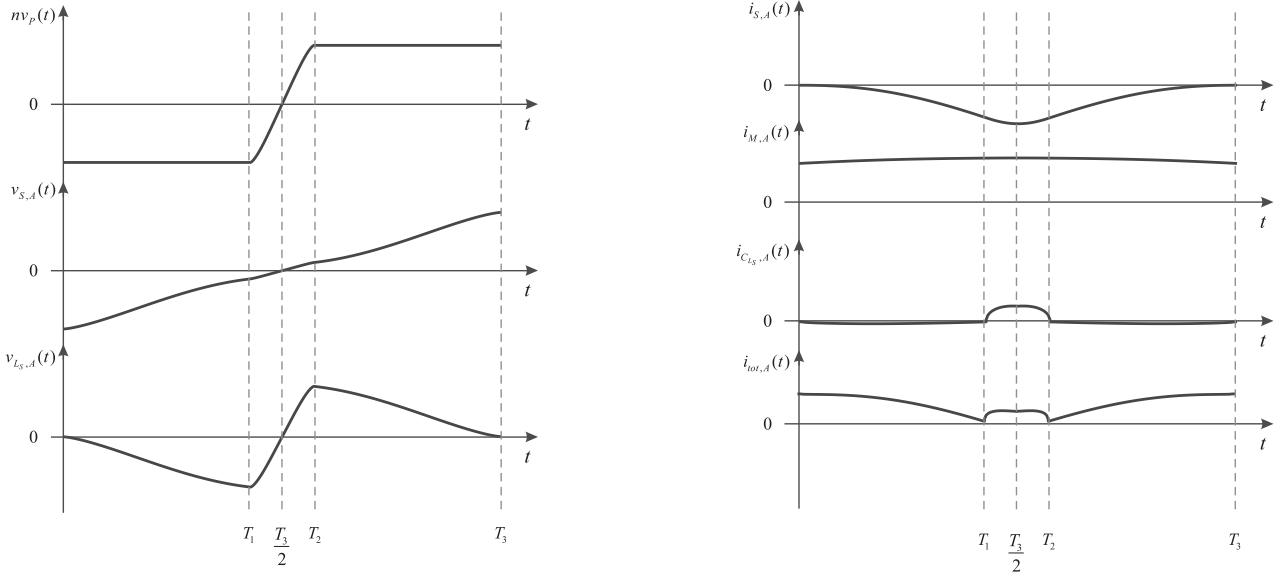


Fig. 4. Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$.

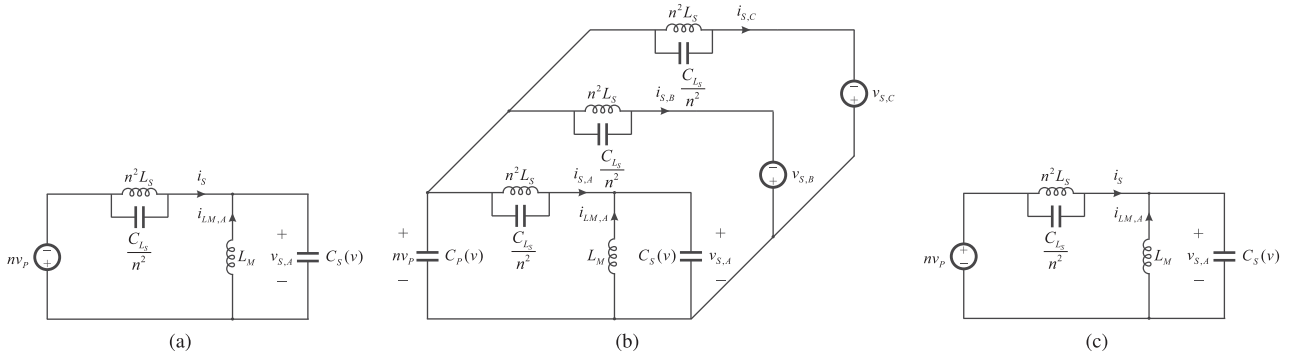


Fig. 5. Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases. (a) Equivalent circuit for Interval I. (b) Equivalent circuit for Interval II. (c) Equivalent circuit for Interval III.

as described above. Fig. 4 shows theoretical waveforms for the case when the minimum of $i_{tot,A}$ is zero. This represents the optimal design, in the sense of achieving ZVS operation while minimizing the peak of the magnetizing inductance current, and therefore, minimizing the conduction losses introduced by the circulating current.

III. PARAMETER SELECTION FOR MINIMUM PEAK MAGNETIZING CURRENT

In order to achieve ZVS at zero power transfer, the following circuit parameters need to be determined.

- 1) Primary dead time: t_{dp} .
- 2) Secondary dead time: t_{ds} .
- 3) Magnetizing inductance referred to the secondary side: L_M .

In the design approach detailed in this section, all the parameters are expressed in terms of the specifications and the circuit parameters shown in Table III. In this section, the maximum phase shift φ_m is considered to be a known input parameter. The optimal value of φ_m , and the corresponding optimal value

TABLE III
SYSTEM SPECIFICATIONS AND CIRCUIT PARAMETERS

P	Rated power
V	DC link voltage
n	Transformer turns ratio
f_{sw}	Switching frequency
φ_m	Maximum phase shift

of the series inductance, are found in Section IV to minimize the total loss in the module.

The series inductance

$$L_S = \frac{3V^2\varphi_m \left(1 - \frac{\varphi_m}{\pi}\right)}{4\pi n^2 f_{sw} P} \quad (3)$$

and the peak value of the primary side current

$$I_{P,pk} \approx \frac{nP}{V \left(1 - \frac{\varphi_m}{\pi}\right)} \quad (4)$$

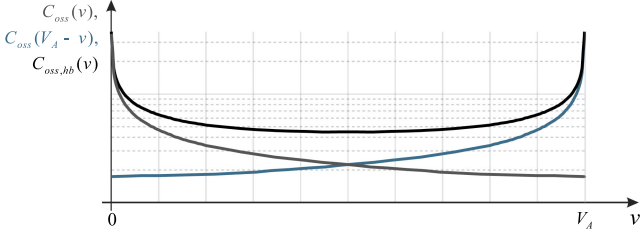


Fig. 6. Half-bridge switching node device capacitance.

are found using the standard steady-state solution for the active-bridge converters [9].

A. Nonlinear Switching Node Capacitance

In the small-signal sense, capacitance at the half-bridge switching node is a parallel combination of the two device output capacitances, $C_{oss,hb}(v) = (C_{oss}(v) + C_{oss}(V_A - v))$, as shown in Fig. 6, where $C_{oss}(v)$ curve can be found from the device datasheet, and V_A is the dc voltage across the half bridge. The total half-bridge switching node capacitance is a combination of the device capacitances, series inductor and transformer winding capacitance, and the parasitic PCB trace capacitance. The half-bridge capacitances of the primary and the secondary side, denoted as $C_{P,hb}(v)$ and $C_{S,hb}(v)$, respectively, can be found as

$$C_{P,hb}(v) = C_{oss,hb,P}(v) + 2(3C_{L_s} + C_{PCB,P}) \quad (5)$$

$$C_{S,hb}(v) = C_{oss,hb,S}(v) + 2\left(\frac{C_{tr}}{n^2} + C_{PCB,S}\right). \quad (6)$$

It should be noted that C_{L_s} has been left out of $C_{S,hb}(v)$, since this capacitance will be treated separately from the rest of the lumped secondary-side capacitances. For the equivalent circuit representation used in Figs. 5 and 7, it is convenient to define full-bridge switching-node voltage-dependent capacitances as $C_P(v) = C_{P,hb}(v)/2$ for the primary side, and $C_S(v) = C_{S,hb}(v)/2$, for the secondary side.

The energy and charge equivalent primary-side full-bridge switching-node capacitance are found, respectively, as follows [23]:

$$C_{P,E} = \frac{n^2 \int_0^{\frac{V}{n}} v C_{P,hb}(v) dv}{V^2} \quad (7)$$

$$C_{P,Q} = \frac{n \int_0^{\frac{V}{n}} C_{P,hb}(v) dv}{2V}. \quad (8)$$

The analysis in Section III-C considers only one half of the secondary side ZVS transition. More precisely, the secondary side ZVS analysis is divided into two segments. In the first segment ($0 \leq t < T_1$), the energy equivalent secondary-side full-bridge switching-node capacitance $C_{S,I}$ is obtained by integration up to V'

$$C_{S,I} = \frac{\int_0^{V'} v (C_{S,hb}(v) + 2C_{L_s}) dv}{V'^2} \quad (9)$$

where V' is equal to one half of the dc link voltage reduced by the half of the $v_{S,A}$ increase during the second segment

($T_1 \leq t < T'_1$). A more detailed derivation of V' is addressed in Section III-C.

During the second segment, $v_{S,A}$ is approaching one half of the dc link voltage, resulting in a relatively flat nonlinear capacitance, as illustrated in Fig. 6. Therefore, the secondary-side full-bridge switching-node capacitance $C_{S,II}$ during the second segment can be obtained simply as

$$C_{S,II} = C_{S,hb}(0.5V) + 2C_{L_s}. \quad (10)$$

B. Primary Side Dead Time

Since the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much greater than $i_{M,A}$, the rise time of the primary side switching node can be analyzed neglecting the effect of the phase A secondary side current $i_{S,A}$. Therefore, the equivalent circuit in Fig. 5(b) can be reduced to a simple LC circuit. The charge equivalent capacitance can be used to accurately calculate the switching-node voltage rise time, under the assumption that the energy stored in the series inductor is much larger than the energy used for charging the switching-node capacitance

$$I_{P,pk} \gg \frac{2V}{n} \sqrt{\frac{C_{P,E}}{L_s}}. \quad (11)$$

Consequently, the primary-side dead time t_{dp} can be found as

$$t_{dp} = \frac{2VC_{P,Q}}{nI_{P,pk}} = \frac{2C_{P,Q}V^2}{n^2P} \left(1 - \frac{\varphi_m}{\pi}\right). \quad (12)$$

C. Magnetizing Inductance and Secondary-Side Dead Time

The switching sequence, described in Section II, involves equivalent circuits shown in Fig. 7. An exact solution is complicated for two reasons: nonlinear nature of the switching-node capacitances, and multiresonant responses, especially in Interval II. An approximate, design-oriented analytical approach is developed in this section to arrive at relatively simple, yet accurate design guidelines for the selection of the magnetizing inductance L_M and the secondary-side dead-time t_{ds} . The following approximations are applied in order to simplify the equivalent circuits in Fig. 5 and arrive at the approximate equivalent circuits in Fig. 7.

- 1) Since the primary side switching node voltage exhibits an approximately linear rise, the C_{L_s} branch current is approximated with a constant current source $I_{C_{L_s}}$ in Interval II (between T'_1 and T'_2), as shown in Fig. 8.
- 2) The primary-side switching-node voltage v_P is approximated by a stair-step waveform during Interval II, as shown in Fig. 8. The approximation is justified by the fact that Interval II is relatively short compared to the overall ZVS transition time, and details of $nv_P(t)$ transitioning from 0 to V have little impact on the secondary-side ZVS transition waveforms. Furthermore, the approximate stair-step waveform is symmetric around the mid-point of the transition, which also simplifies the analysis.
- 3) The magnetizing inductance current is considered constant and equal to I_M during the ZVS transition. This is justified by the fact that the magnetizing inductance is much larger than the series inductance, so that

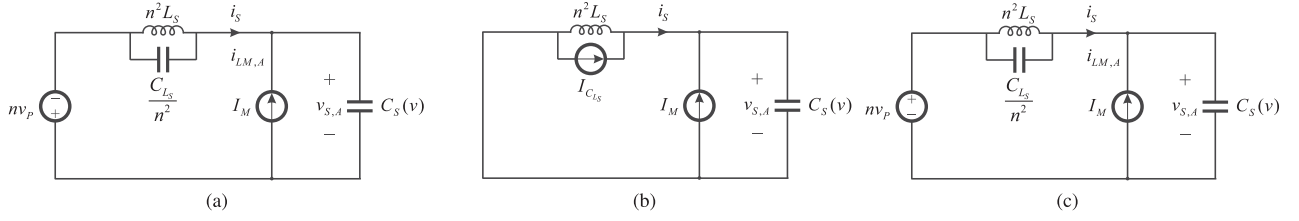


Fig. 7. Approximate equivalent circuits during ZVS transition. (a) Equivalent circuit for Interval I'. (b) Equivalent circuit for Interval II'. (c) Equivalent circuit for Interval III'.

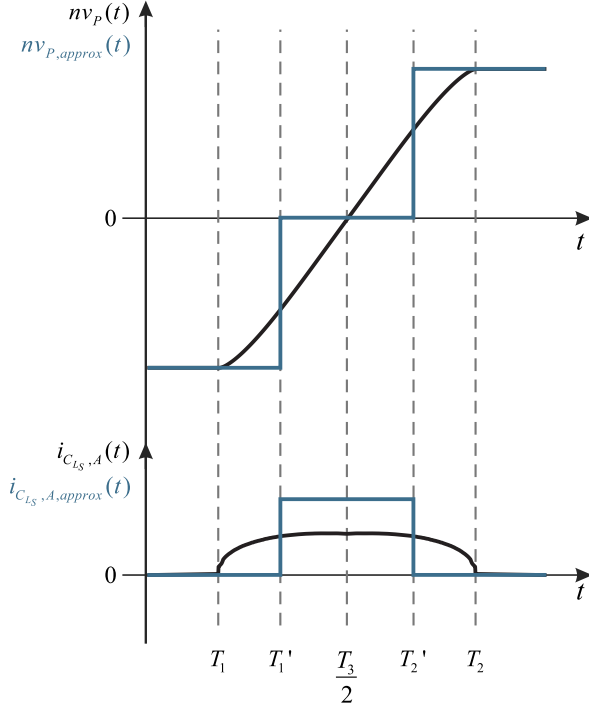


Fig. 8. Exact and approximate waveforms of the primary-side switching-node voltage $nv_p(t)$ during Interval II.

TABLE IV
TIME INSTANTS OF THE APPROXIMATED
SWITCHING SEQUENCE

T_1'	$0.5(t_{ds} - 0.5t_{dp})$
T_2'	$0.5(t_{ds} + 0.5t_{dp})$
T_3'	t_{ds}

TABLE V
TIME INTERVALS OF THE APPROXIMATED
SWITCHING SEQUENCE

Interval I'	$0 \leq t < T_1'$
Interval II'	$T_1' \leq t < T_2'$
Interval III'	$T_2' \leq t < T_3'$

variations in i_M are relatively small during the ZVS transition.

The approximate equivalent circuits of the ZVS switching sequence are shown in Fig. 7. Definitions of the time instants and time intervals corresponding to the approximate switching sequence are given in Tables IV and V. The approximations greatly

reduce complexity of the analysis, simplifying the switching sequence states to second-order circuits well suited for state-plane analysis. Since the switching sequence and the waveforms are symmetrical around $T_3/2$, as shown in Fig. 4, it is sufficient to perform the analysis over one half of the ZVS transition, from 0 to $T_3/2$.

The secondary side half-transition can be divided into two intervals as follows.

- 1) Interval I' [approximate equivalent circuit is shown in Fig. 7(a)]; in order to achieve ZVS with a minimum magnetizing current, i_{tot} should drop to zero at T_1' , as discussed in Section II. Equivalently, $i_{S,A}$ should drop to $-I_M$. At this point, $v_{S,A}$ reaches $-\Delta V_{S,A}$.
- 2) First half of interval II' [approximate equivalent circuit shown in Fig. 7(b)]; with the help of $I_{C_{L_S}}$, the secondary-side voltage rises by $\Delta V_{S,A}$, and reaches zero in the middle of Interval II'.

For state-plane analysis of the circuit in Fig. 7(a) and (b), the normalized voltage and current can be written as

$$m_{S,A} = \frac{v_{S,A}}{V_{base}}$$

$$j_{S,A} = \begin{cases} \frac{i_{S,A}}{I_{base,I}} & \text{for Interval I} \\ \frac{i_{S,A}}{I_{base,II}} & \text{for Interval II} \end{cases} \quad (13)$$

where

$$V_{base} = V, \quad I_{base,I} = \frac{V_{base}}{R_{0,I}}, \quad I_{base,II} = \frac{V_{base}}{R_{0,II}} \quad (14)$$

and

$$R_{0,I} = n\sqrt{\frac{L_S}{C_{S,I}}}, \quad R_{0,II} = n\sqrt{\frac{L_S}{C_{S,II}}} \quad (15)$$

The resulting state-plane trajectory is shown in Fig. 9. A discontinuity can be observed in $j_{S,A}$ because the two intervals have two different base currents. On the other hand, since R_0 does not affect the voltage normalization, m_S remains continuous.

Since the analysis of Interval I' requires the knowledge of $\Delta V_{S,A}$, Interval II' is considered first.

1) Interval II': Given the approximation that the primary side switching-node voltage v_P is increasing linearly, and that the secondary side switching-node voltage $v_{S,A}$ does not change much compared to v_P , current $I_{C_{L_S}}$ can be found

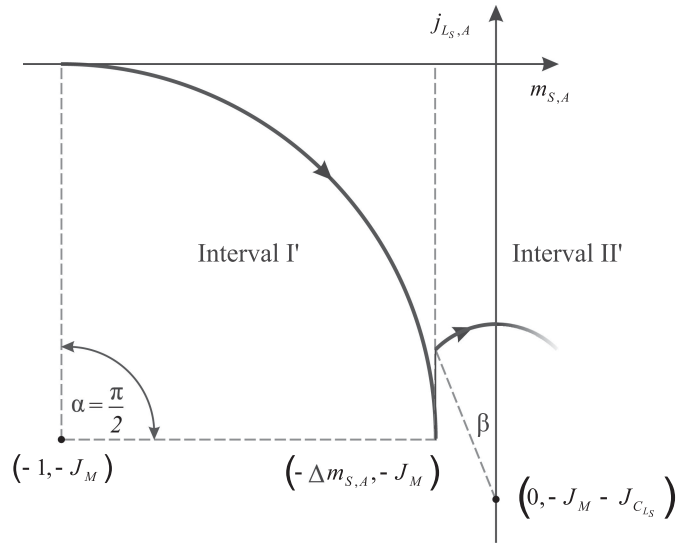


Fig. 9. State plane trajectory during intervals I' and II'.

approximately as

$$I_{C_{LS}} = \frac{2VC_{LS}}{n^2 t_{dp}} \quad (16)$$

which in normalized form becomes

$$J_{C_{LS}} = \frac{nI_{C_{LS}}}{V} \sqrt{\frac{L_S}{C_{S,II}}} \quad (17)$$

Angle β is

$$\beta = \frac{t_{dp}}{4n\sqrt{L_S C_{S,II}}} \quad (18)$$

and $\Delta m_{S,A}$ is found as

$$\Delta m_{S,A} = J_{C_{LS}} \tan(\beta) \quad (19)$$

which yields

$$\Delta V_{S,A} = nI_{C_{LS}} \sqrt{\frac{L_S}{C_{S,II}}} \tan\left(\frac{t_{dp}}{4n\sqrt{L_S C_{S,II}}}\right) \quad (20)$$

It is convenient to define V' as

$$V' = \frac{1}{2}(V - \Delta V_{S,A}) \quad (21)$$

This V' has been used as the integration limit in (9) to determine $C_{S,I}$.

2) *Interval I'*: In order for the normalized voltage to reach $-\Delta m_{S,A}$, while the normalized current drops to $-J_M$, the following condition must be met:

$$J_M = 1 - \Delta m_{S,A} \quad (22)$$

The required amplitude of the magnetizing current can be found from (20) and (22)

$$I_M = \left(1 - \frac{\Delta V_{S,A}}{V}\right) \frac{V}{n} \sqrt{\frac{C_{S,I}}{L_S}} \quad (23)$$

and the required magnetizing inductance is

$$L_M = \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds} - t_{dp} \right) \quad (24)$$

where t_{dp} can be found from (12). It remains to determine the secondary-side dead time t_{ds} .

Since the energy stored in the magnetizing inductance is just enough to discharge the switching node capacitance, the charge equivalent linear capacitance cannot be used to determine the secondary-side dead time. The rise time of the secondary side switching node can be estimated more accurately by solving the circuit in Fig. 7(a)

$$t_{ds} = \frac{t_{dp}}{2} + 2 \int_0^{V'} \frac{C_s(v_x) dv}{\sqrt{I_M^2 - \frac{4}{n^2 L_S} \int_0^v C_s(v_x) v_x dv_x}} \quad (25)$$

where

$$C_s(v_x) = C_{S,hb}(v_x) + 2C_{L_S} \quad (26)$$

This result can be used to properly set the dead time in a practical implementation. With the goal of arriving at a simpler, closed-form solution for the required magnetizing inductance, it should be noted that the impact of t_{ds} in (24) is relatively small. An approximate expression for t_{ds} can therefore, be found from the state-plane analysis illustrated in Fig. 9 by noting that T'_1 interval corresponds to angle $\alpha = \pi/2$

$$\alpha = \frac{T'_1}{n\sqrt{L_S C_{S,I}}} = \frac{\pi}{2} \quad (27)$$

using the energy-equivalent secondary-side capacitance $C_{S,I}$ evaluated over one half of the dc link voltage. Given that $T'_1 = 0.5(t_{ds} - 0.5t_{dp})$, (27) yields an approximate expression for the secondary-side dead time

$$t_{ds,approx} = \frac{t_{dp}}{2} + \pi n \sqrt{L_S C_{S,I}} \quad (28)$$

where L_S and t_{dp} can be found from (3) and (12), respectively.

Finally, an approximate closed-form expression for the required magnetizing inductance L_M follows from (24):

$$L_M \approx \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds,approx} - t_{dp} \right) \quad (29)$$

where, in terms of the circuit specifications and parameter values, t_{dp} can be found from (12), I_M from (23), and $t_{ds,approx}$ from (28).

D. Sensitivity to Parameter Variations

The analysis and the design guidelines presented in this section depend on the circuit parameter values, specifically the switching node capacitance and the series inductance. A sensitivity analysis with respect to ΔL is performed for the converter prototype specifications given in Section V. Fig. 10 shows how a percent variation ΔL in the series inductance affects relative changes in the resulting design parameters Δt_{sd} and ΔL_M . With respect to both design parameters, a relatively low sensitivity of approximately 0.5 is observed. Furthermore, given the approximation (12) used to determine the primary-side

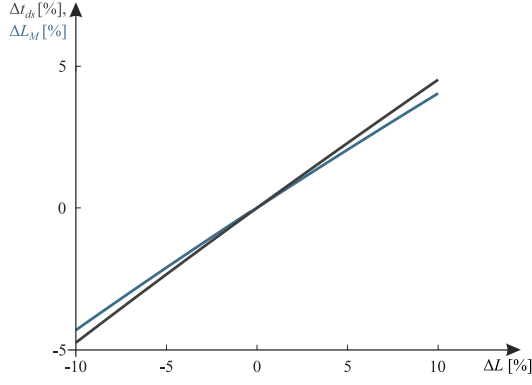


Fig. 10. Effects of the variation in the series inductance on the changes Δt_{sd} and ΔL_M in the design parameters.

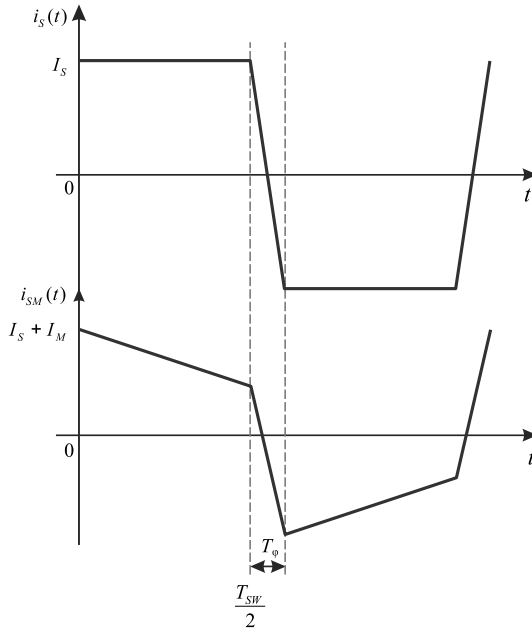


Fig. 11. Theoretical currents waveforms during a switching period.

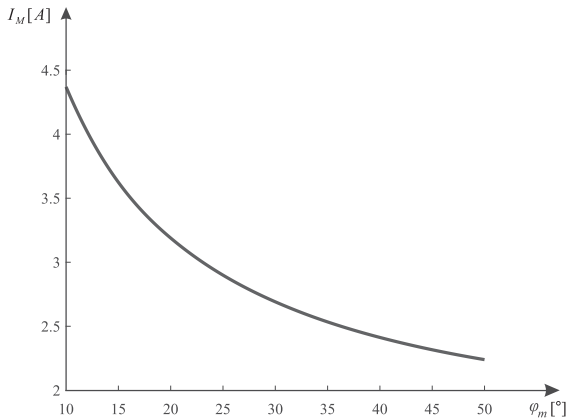


Fig. 12. Peak magnetizing current dependence on φ_m .

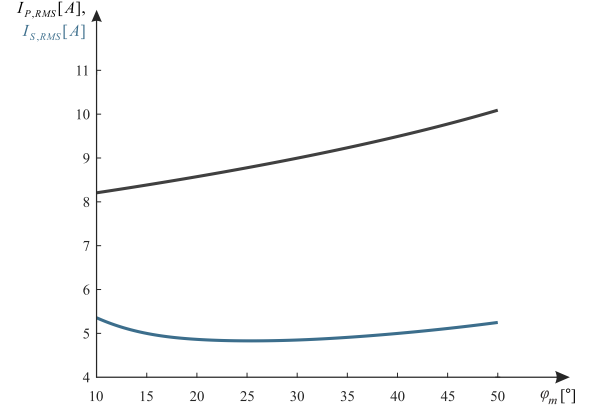


Fig. 13. RMS primary and secondary currents as functions of φ_m .

TABLE VI
EXPERIMENTAL PROTOTYPE PARAMETERS

P	V	n	f_{sw}
10 kW	1 kV	1	200 kHz

TABLE VII
CAPACITANCES IN THE EXPERIMENTAL PROTOTYPE

C_{tr}	C_{L_s}	C_{PCB}	$C_{P,Q}$	$C_{S,I}$	$C_{S,II}$
265 pF	55 pF	35 pF	497 pF	606 pF	526 pF

deadtime, this design parameter is not affected significantly by the variation in series inductance.

IV. DESIGN OPTIMIZATION

For a given series inductance L_S , and the corresponding maximum phase shift φ_m , the design approach described in Section III minimizes the magnetizing current required to achieve ZVS at all times. In this section, major loss mechanisms, including semiconductor conduction losses, as well as core and conduction losses in the magnetics, are analyzed as functions of the maximum phase shift, and the optimum values of φ_m and L_S are found to minimize the losses.

The case study is a 10 kW, 1-kV QAB stage, with the specifications summarized in Table VI. The MOSFETs are 1700-V SiC (Wolfspeed Cree C2M0045170P). Values of the parasitic capacitances that are important for the minimum peak magnetizing current calculation are shown in Table VII. The optimization is carried out at 75% of the full load, since this load has the highest weight in the CEC efficiency calculation [24].

A. Active-Bridge Conduction Losses

Since the input average current is constant, the primary side rms current $I_{PR,RMS}$ can be calculated simply by integrating the trapezoidal current waveform with the peak value given by (4)

$$I_{PR,RMS} = \left(\frac{P}{V}\right) \frac{\sqrt{\left(1 - \frac{2\varphi_m}{3\pi}\right)}}{\left(1 - \frac{\varphi_m}{\pi}\right)}. \quad (30)$$

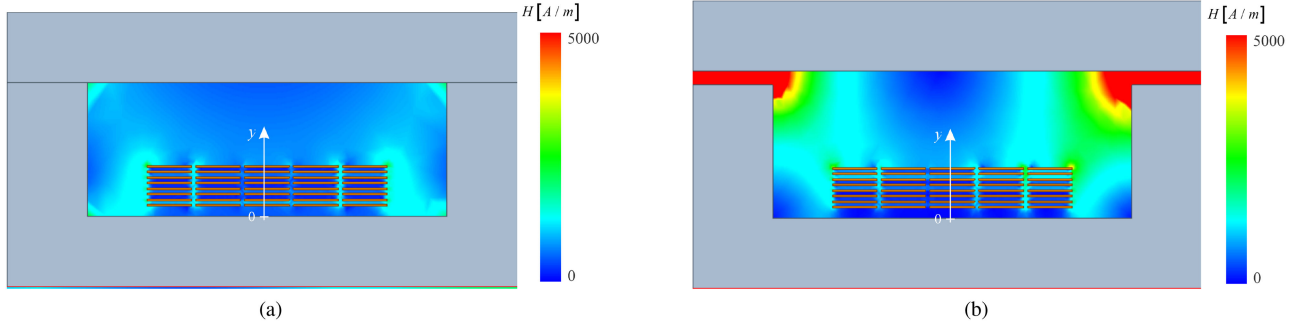


Fig. 14. 2-D FEA simulation showing H field distribution in the planar high frequency transformer at a point of the line cycle. (a) Without the air gap. (b) With the air gap.

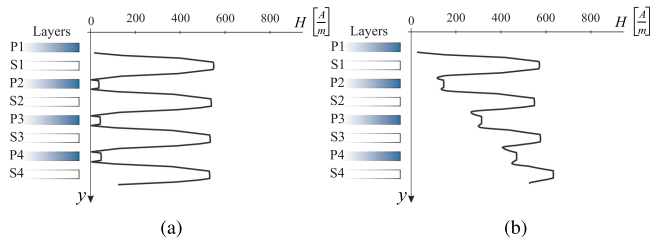


Fig. 15. H field magnitude in the planar high frequency transformer along y axis at one instant during a line cycle. (a) Without the air gap. (b) With the air gap.

Secondary-side current waveshapes $i_S(t)$ and $i_{SM}(t) = i_S(t) + i_M(t)$ are shown in Fig. 11. It is important to note that the phase shift φ and the amplitude I_S vary over a half line period

$$I_S(t) = \frac{2P}{3V \left(1 - \frac{\varphi(t)}{\pi}\right)} \quad (31)$$

while the peak I_M of the magnetizing current can be found from (23).

Secondary rms current $I_{SEC,RMS}$ can be found by first calculating the secondary rms current over a switching period $i_{SM,RMS}(t)$ based on the waveforms shown in Fig. 11 and the expressions for I_S and I_M , and then by integration over the line cycle. The peak of the magnetizing current and the primary and the secondary rms currents are shown in Figs. 12 and 13 as functions of φ_m . It can be noted that I_M decreases as φ_m increases. This is because a higher φ_m implies a large L_S , and a smaller magnetizing current is, therefore, required to achieve the ZVS sequence described in Section II. Following the trend in DAB converters [25], the primary-side rms current increases as φ_m increases because of the larger reactive component of the series current. The secondary-side rms current has both magnetizing and series current components, which is why $I_{SEC,RMS}$ is a convex function of φ_m .

The primary-side active-bridge conduction loss is given by

$$P_{cond,PR} = 2R_{on,PR} \left(\frac{P}{V}\right)^2 \frac{\left(1 - \frac{2\varphi_m}{3\pi}\right)}{\left(1 - \frac{\varphi_m}{\pi}\right)^2} \quad (32)$$

and the secondary-side active-bridge conduction loss can be found by integration over a line cycle

$$P_{cond,SEC} = 6R_{on,SEC} I_{SEC,RMS}^2 \quad (33)$$

B. Loss in the Magnetic Components

The high-frequency transformer is a critical component, since the converter module is intended for the system architecture in Fig. 1, where the transformer needs to withstand medium voltage (MV) between primary and secondary windings. Planar technology is chosen for magnetics implementation because of the ease of manufacturability and repeatability [26]–[28].

The transformer design is based on two side-by-side EILP 102 cores, with 20 turns per winding on four PCB layers using 5-Oz copper. The primary and secondary layers are interleaved. The required MV isolation is achieved using polyimide dielectric (instead of standard FR4) between the PCB layers and by keeping sufficient spacing between the copper traces, the vias, and the core, as described in more detail in [29]. The MV isolation requirement results in significantly longer and narrower traces in the transformer, which leads to higher dc resistance, and, thereby increased winding losses.

Increasing the magnetizing current is achieved by insertion of an air-gap in the transformer core, which does not affect the core loss but affects the transformer winding loss significantly. To minimize proximity effects, the primary and secondary winding layers are interleaved. However, as illustrated by finite-element analysis (FEA) simulation results in Fig. 14, with the air-gap, the H -field distribution has significantly larger intensity around the top layers of the transformer windings. Fig. 15 shows 2-D plots of the $|H(y)|$ dependence, without and with the air-gap. With the air-gap [Fig. 15(b)], the H -field increases progressively through the layers. This is because the currents through the primary and the secondary side of the transformer are not perfectly balanced (see Fig. 11), which results in increased proximity losses compared to the case of perfect interleaving between the primary and the secondary layers illustrated in Fig. 15(a).

Since standard analytical methods [30] do not apply to gapped transformers, where the magnetizing current is significant, a more general method is used to accurately predict the loss in the windings. As discussed in [31], for arbitrary relationships between the magnitude and phase of the primary and secondary currents, the transformer winding loss can be found using a

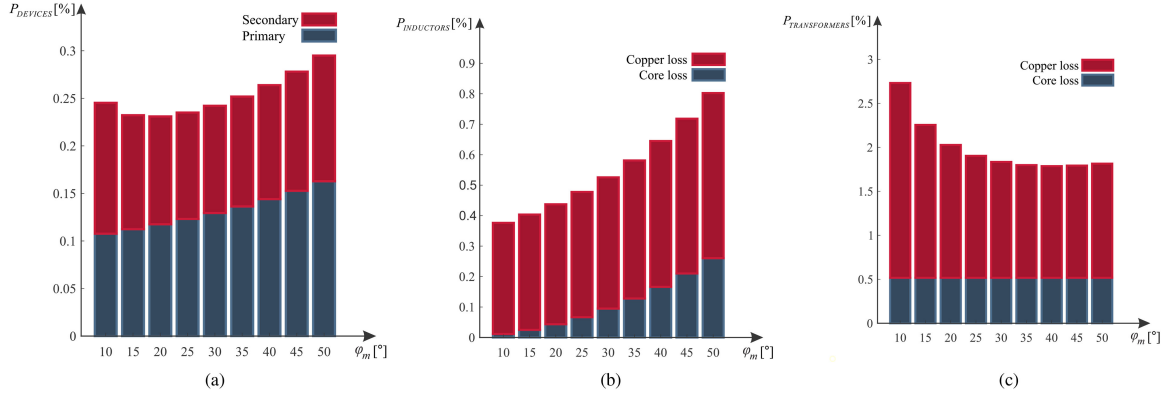


Fig. 16. Component losses as functions of the maximum phase shift φ_m . (a) Conduction loss in the devices. (b) Loss in the inductors. (c) Loss in the transformer.

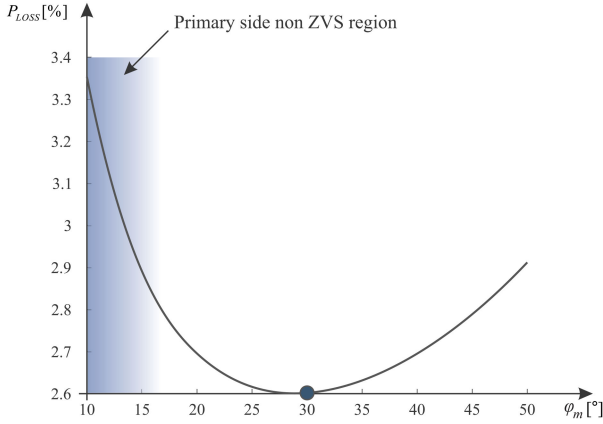


Fig. 17. Total loss as a function of φ_m .

resistance matrix

$$P_{cu,tfo} = \frac{1}{2} \sum_{\omega} R_{11}(\omega) I_1(j\omega) I_1^*(j\omega) + R_{12}(\omega) (I_1(j\omega) I_2^*(j\omega) + I_2(j\omega) I_1^*(j\omega)) + R_{22}(\omega) I_2(j\omega) I_2^*(j\omega) \quad (34)$$

where $I_1 = I_{S,A}$ and $I_2 = I_{S,A} + I_{M,A}$ are phasors of the currents through primary and secondary windings of the transformer, respectively. Since the currents shown in Fig. 11 have high harmonic content, the losses are calculated up to the tenth harmonic. For example, at 200 kHz, the resistance matrix of the transformer obtained using 3-D FEA (Ansys Maxwell) simulations is

$$\begin{bmatrix} R_{11} & R_{12} \\ R_{12} & R_{22} \end{bmatrix} = \begin{bmatrix} 2.6 \Omega & -2.1 \Omega \\ -2.1 \Omega & 2.6 \Omega \end{bmatrix}. \quad (35)$$

The series inductors are using ELP 64 core, with ten turns of 2-Oz copper in five layers. The ac resistance of the inductor at 200 kHz is

$$R_{ind} = 392 \text{ m}\Omega. \quad (36)$$

In contrast to the transformer winding losses, losses in the series inductors are not affected by the magnetizing current. However, the maximum phase shift affects both the core and

the conduction loss in the inductors. A larger maximum phase shift implies more volt-seconds applied and a larger rms current, therefore, increasing both core and conduction loss, as shown in Fig. 16(b).

C. Total Modeled Loss

Contributions to the loss of each component separately, and the total modeled loss are shown in Figs. 16 and 17, respectively, as functions of the maximum phase shift φ_m as the design parameter. The modeled losses are expressed as percentages of 7.5 kW, which is the power level considered for design optimization.

For small values of φ_m , the required peak of the magnetizing current increases, thus increasing the loss in the secondary-side bridge and the transformer windings. For large values of φ_m , the reactive component in the series current increases, resulting in increased conduction losses. In choosing the optimal value of φ_m , it is further important to take into account the primary-side ZVS condition given by (11). Fig. 17 shows how this constraint restricts the range of considered maximum phase shift above a lower limit for φ_m . The maximum phase shift that minimizes the total loss in the converter is $\varphi_m = 30^\circ$.

V. EXPERIMENTAL RESULTS

The experimental prototype of the dc-to-three-phase ac module is shown in Fig. 18. The prototype specifications are summarized in Table VI, and the component parameters are provided in Table VIII. The prototype consists of one primary board, three secondary boards, and the planar magnetics. The primary and each of the secondary boards have a dedicated microcontroller. Each secondary board includes a secondary-side bridge of the QAB, and an H-bridge inverter, as shown in Fig. 2.

All the communication between the primary and the secondary boards is done through optical cables. The signaling includes: 1) synchronization pulses at $f_s = 200$ kHz from the primary to each of the secondary boards to facilitate the phase-shift control of the QAB, and 2) 60-Hz synchronization pulses used for setting the power reference at the secondaries, which is realized using the controller area network (CAN) protocol.

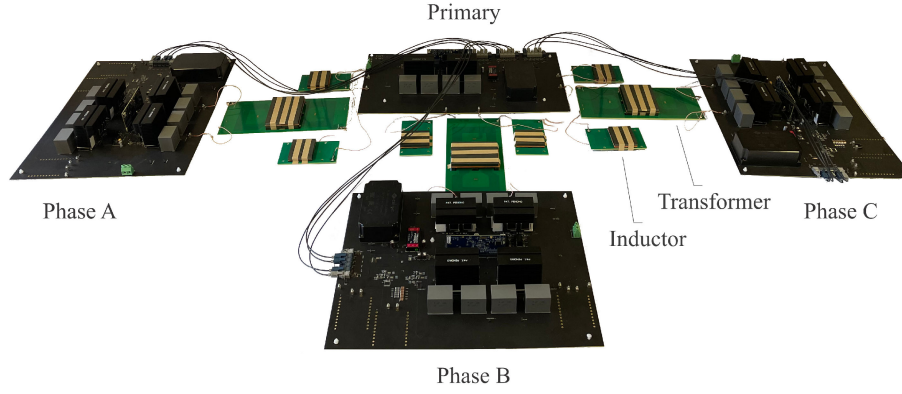
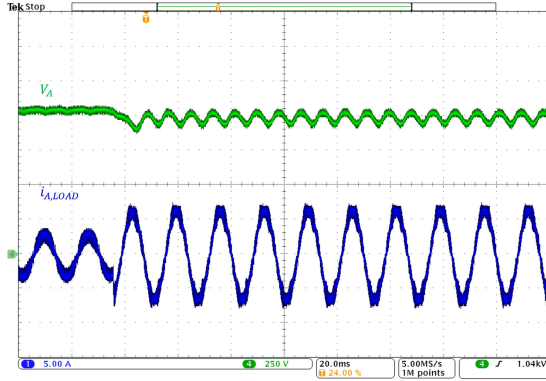


Fig. 18. 1 kV, 10-kW SiC-based prototype of the isolated dc to three-phase ac module.

Fig. 19. Phase A dc-link voltage V_A and the inverter output current $i_{A,LOAD}$, during a step change from 50% to 100% of load.TABLE VIII
COMPONENTS USED IN THE HARDWARE PROTOTYPE

Component	Part number	Details
MOSFET	C2M0045170P	SiC, 1.7 kV, $R_{ds(on)} = 45 \text{ m}\Omega$
Inductor	EILP 64	$n_{\text{turns}} = 10$, $n_{\text{layers}} = 5$, $t_{cu} = 2 \text{ Oz}$, $l_{\text{gap}} = 2.28 \text{ mm}$
Transformer	2 x EILP 102	$n_{\text{turns}} = 20$, $n_{\text{layers}} = 4$, $t_{cu} = 5 \text{ Oz}$, $l_{\text{gap}} = 1.4 \text{ mm}$ $t_{\text{preg}} = 5 \text{ mil (polyimide)}$ $V_{\text{Hipot}} = 26 \text{ kV}$
DC-link cap	8 x C4AQSBW4800A3JJ	$8 \mu\text{F}$ each

To validate dc bus voltage regulation and voltage ripple, Fig. 19 shows a transient response to a 50–100% load step at the inverter output. The PIR controller, designed as discussed in [32], is capable of firmly regulating the output voltage against load transients. Also, as expected, a twice line frequency ripple is visible in the dc-link voltage due to the large output current disturbance at this frequency. However, the dc-link voltage is maintained within relatively narrow limits. At full load the ripple amplitude is 4% of the dc voltage, while at light load it is less than 1%. This validates the assumption that the dc bus voltage can be considered constant in the analysis.

TABLE IX
DEAD TIMES, MAGNETIZING INDUCTANCE, AND MAXIMUM PHASE SHIFT IN THE EXPERIMENTAL PROTOTYPE

t_{dp}	t_{ds}	L_M	φ_m
110 ns	740 ns	385 μH	30°

A. Design Validation

The primary-side dead time is calculated from (12), while the secondary-side dead time and the magnetizing inductance are calculated according to (25) and (29), respectively, and the results are summarized in Table IX. By inserting the air-gap in the transformer, the value of the magnetizing inductance is reduced from 6 mH to 385 μH . The air-gaps inserted in the transformers and the inductors are 1.4 and 2.28 mm, respectively. The peak flux density in the transformer core is 60 mT, which is independent of the instantaneous power level, while the peak flux density in the inductor core varies with the instantaneous power in the range from 0 to 45 mT.

The series inductance is split in two, to provide symmetric impedance in the common-mode path, and thus, reduce common-mode current circulation through the transformer [33], [34].

Fig. 20 shows how the three-phase secondary QAB currents are summing up to a constant-envelope current on the primary side. The waveforms are shown for the currents $i_{S,A}$, $i_{S,B}$, and $i_{S,C}$ in Fig. 20(a), and the currents including the magnetizing currents in Fig. 20(b), which illustrate how the additional circulating currents are relatively small. Fig. 21(a) shows ZVS operation at the zero power crossing of phase A, while Fig. 21(b) confirms that the measured waveforms closely match the theoretical waveforms shown in Fig. 4. It should be noted that the planar implementation of the magnetic components have pronounced parasitics, which result in increased high-frequency parasitic oscillations. For example, Fig. 21(b) shows that there are high-frequency components in $i_{S,A}$ and in $i_{S,A} + i_{M,A}$ due to resonance between the parasitic capacitance of the series inductors and the leakage inductance of the transformer. Aside from high-frequency effects, however, the waveforms in fact demonstrate very good match with the model.

In order to verify the approximations introduced in Section III-C, two model-based simulations are performed, and

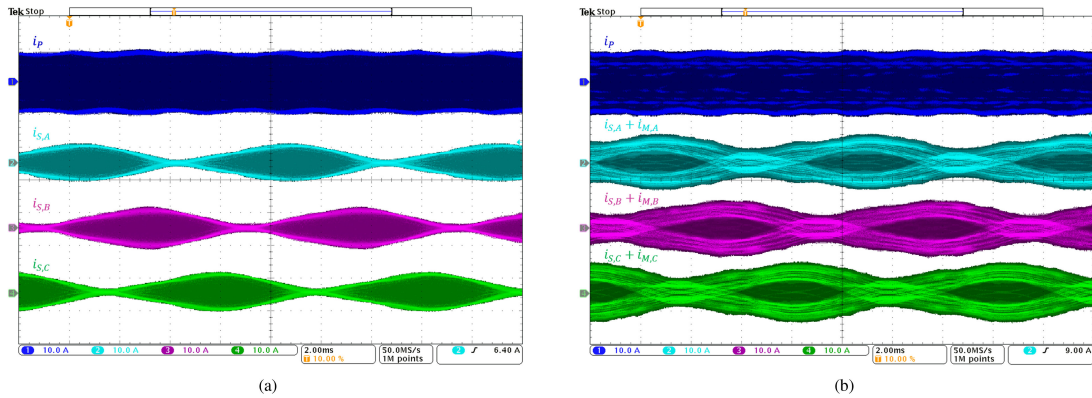


Fig. 20. Quadruple active bridge primary and secondary currents. (a) Primary current i_P , and secondary currents through L_S . (b) Primary current i_P , and secondary currents through L_S and L_M .

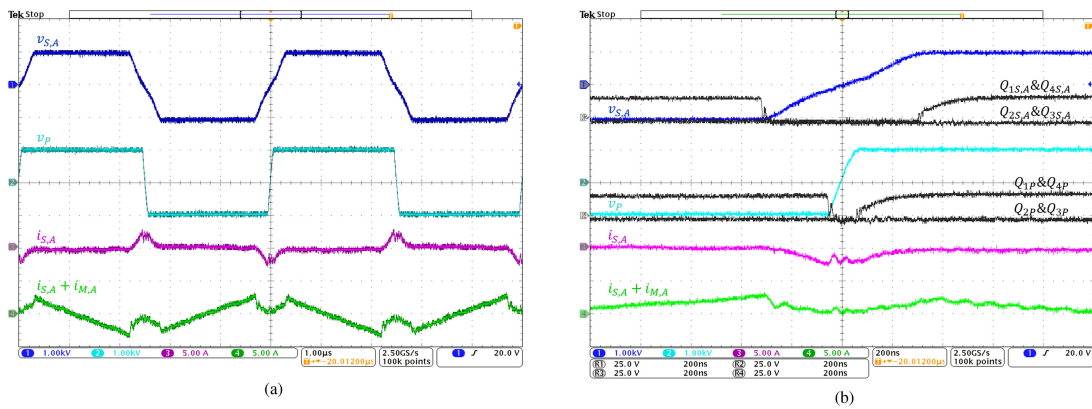


Fig. 21. Waveforms illustrating zero voltage switching at the zero power instant for phase A. (a) Switching-node voltages $v_{S,A}$, v_P , and currents $i_{S,A}$ and $i_{S,A} + i_{M,A}$. (b) Waveforms during ZVS transition.

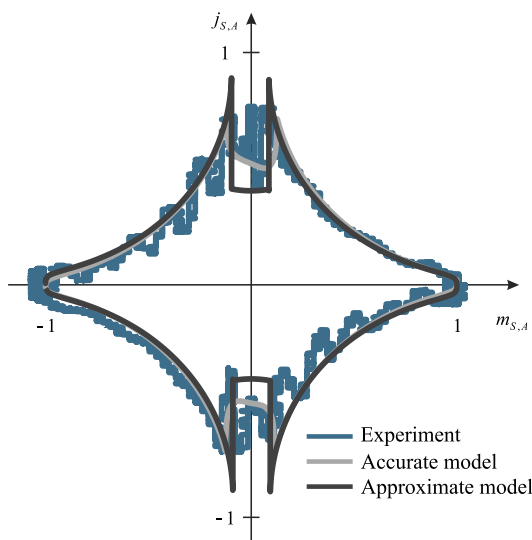


Fig. 22. State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.

compared with the experimental results. An accurate model is developed based on the equivalent circuits shown in Fig. 5. A simpler model, which is used to derive design equations in Section III, is based on the equivalent circuits shown in

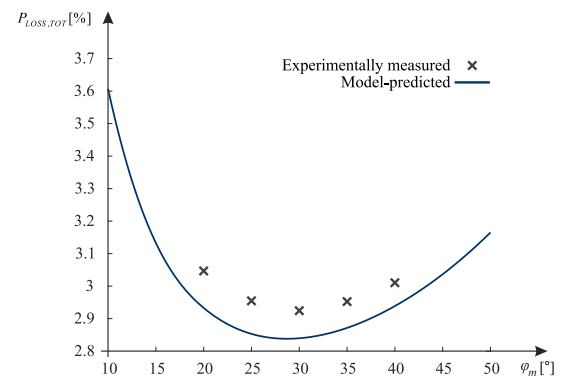


Fig. 23. Experimentally measured loss for designs around the optimum φ_m together with the model-predicted optimization curve.

Fig. 7. Fig. 22 shows a good agreement between the state-plane trajectories obtained from the accurate model, the approximate model, and the experimental waveforms.

The optimization carried out in Section IV is validated experimentally by testing different designs around the optimum φ_m point. Each of the measured data points corresponds to different transformer and inductor air-gaps adjusted around the values obtained by the model-based optimization. As Fig. 23 shows,

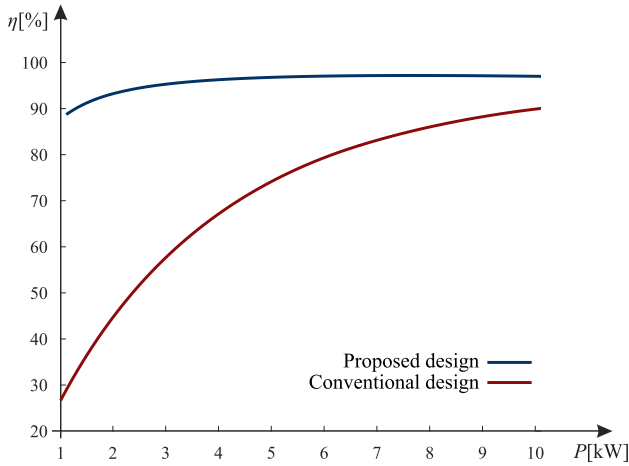


Fig. 24. Model-predicted efficiency curves for the design with the optimized maximum phase shift, magnetizing inductance, and dead times, and for the conventional design with ungapped transformers.

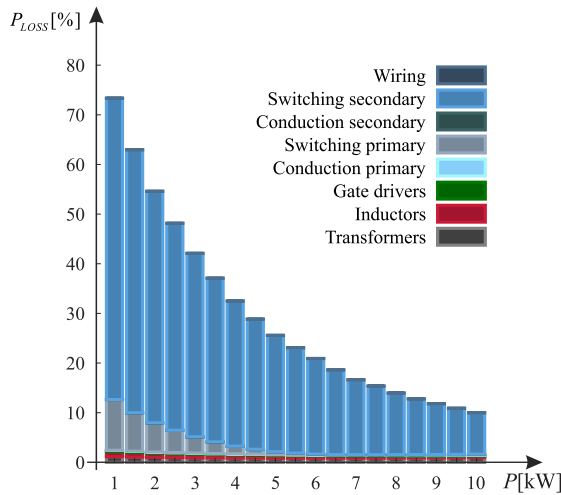


Fig. 25. Model-predicted loss breakdown of the QAB prototype using conventional design with ungapped transformers.

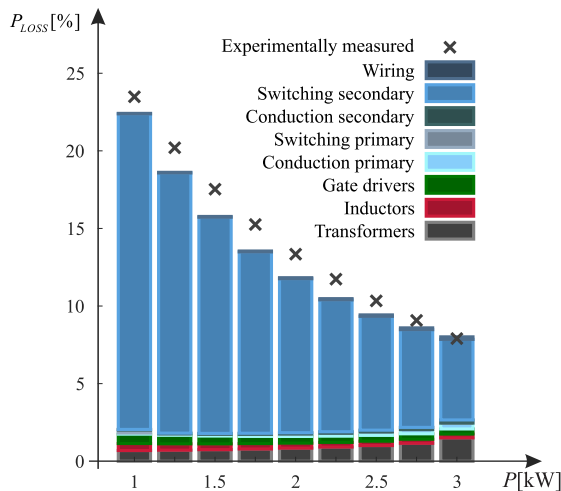


Fig. 26. Loss of the experimental QAB prototype operating at 500-V dc link voltages using conventional design with ungapped transformers, together with a model-predicted loss breakdown.

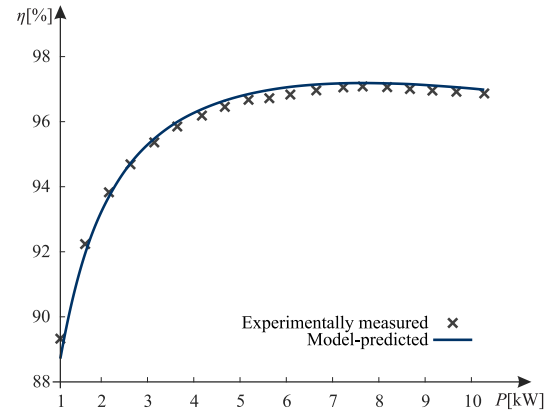


Fig. 27. Efficiency of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted efficiency curve.

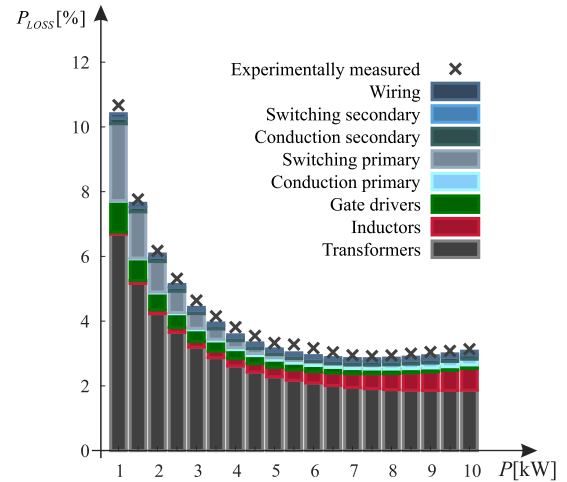


Fig. 28. Loss of the experimental QAB prototype using the optimized maximum phase shift, magnetizing inductance, and dead times, together with a model-predicted loss breakdown.

the experimentally measured optimal φ_m matches the model-predicted value. Additionally, the measured points around the minimum follow the trend of the model-predicted curve.

B. Efficiency Comparison Against a Conventional Design Using a Large Magnetizing Inductance

When the same prototype is operated with a transformer without the air-gaps, while keeping all other parameters the same, switching losses on the secondary-side devices are excessively large, which results in much reduced efficiency. Due to thermal limitations, it is not possible to operate the prototype without the transformer air-gaps at full voltage and power. To illustrate the advantage of the proposed design methodology over the conventional design with ungapped transformers, the model-based efficiency curves are compared in Fig. 24. One may note that the additional loss incurred due to the circulating currents in the gapped-transformer design is much smaller than the secondary-side switching loss in the conventional ungapped-transformer design. As expected, the benefit of the proposed

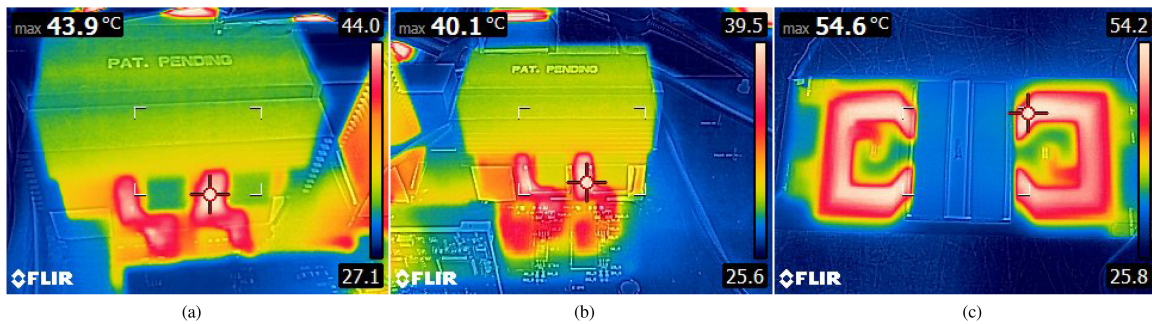


Fig. 29. Thermal images of the devices and one of the transformers in the experimental prototype operating at full power (10 kW) and at room ambient temperature, without any forced-air cooling. (a) Primary-side MOSFETs. (b) Secondary-side MOSFETs. (c) Transformer.

design is particularly visible at lower average power levels, where the energy provided by the series inductance, in the conventional design, becomes insufficient to achieve ZVS over a larger portion of the line cycle. However, even at high load there is an efficiency improvement because the benefits of soft switching over the entire line cycle outweigh the conduction-loss penalty introduced by the extra magnetizing current.

Fig. 25 shows that, in the conventional design, the majority of the loss comes from hard switching of the SiC devices, especially at lighter loads. The switching loss of the secondary-side devices is excessively high because the switching-node capacitance includes the significant interwinding capacitance of the transformer with MV isolation, in addition to the device and PCB capacitances. Furthermore, the dc bus voltage (1 kV) and the switching frequency (200 kHz) are relatively high.

To validate the predicted loss of the conventional design, an experiment is conducted at a reduced voltage of 500 V, over a wide load range. Fig. 26 shows the loss breakdown, which demonstrates a good match with the experimentally measured total loss. The results confirm validity of the loss model and the fact that the switching losses dominate in the conventional design with ungapped transformers.

C. Efficiency and Loss Breakdown

Measured efficiency of the prototype converter is shown in Fig. 27 as a function of the average output power. The efficiency curve is relatively flat, with a peak efficiency of 97.1% at the output power of 7.5 kW, where the design is optimized. The converter efficiency is measured by the Yokogawa Precision Power Analyzer WT3000. The power analyzer has built-in analog low-pass filters, which enable highly accurate sampling of the dc and fundamental frequency components [35].

The model-based loss breakdown, together with the measured loss, are shown in Fig. 28, over a wide load range. A good match is obtained between the predicted and the measured loss. The largest portion of the loss is taken by the high-frequency transformers, due to the MV isolation requirements and the additional winding loss incurred by the circulating currents, as elaborated in Section IV-B.

Fig. 29 shows thermal images of the power devices and the transformer in the experimental prototype operating at full power and at room ambient temperature, without any forced-air cooling.

VI. CONCLUSION

This article presents the design of a QAB converter operating as a fixed-ratio DCX in an isolated dc to three-phase ac module intended for MV modular system architectures. The QAB stage produces three isolated dc link voltages, which serve as inputs for three single-phase dc-to-ac inverter stages. The QAB employs simple phase shift to regulate the dc link voltages. Assuming a balanced three-phase system, the QAB primary-side power is constant, but each secondary side processes time-varying power having a component at twice the line frequency, which makes it difficult to maintain ZVS in the secondary-side active bridges during low-power portions of the line cycle. By placing an airgap into the high-frequency transformer cores, the transformer magnetizing current is increased to achieve ZVS throughout the line cycle. A detailed analysis of the switching transient is presented, including effects of the nonlinear device capacitances and series-inductor parasitic capacitances. Suitable approximations are introduced to obtain closed-form, design-oriented expressions for the magnetizing inductance, and the primary-side and secondary-side dead times, so that ZVS can be achieved, while minimizing the magnetizing current. Furthermore, loss models are developed to enable the system design optimization using the maximum phase shift as a design parameter. An optimum maximum phase shift, series and magnetizing inductances, and dead-times are found to minimize the total loss in the converter.

The proposed approach and the design optimization strategy show significant loss reduction compared to the conventional design with an ungapped transformer. The approach is particularly well suited for higher voltage applications, where hard switching losses can be significant. The method would be less beneficial in lower frequency, lower voltage, or higher current applications, where conduction losses dominate. Experimental results on a SiC-based 1 kV, 10 kW prototype operating at 200 kHz verify the developed models and the optimization approach. The prototype has a relatively flat efficiency curve with the peak efficiency of 97.1% at 7.5 kW.

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