Ajinkya Ajit Phanse

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Research Interests

Component and System-level Power Electronics, High-frequency Magnetics, Analog and Power Management ICs

Education

THE UNIVERSITY OF TEXAS AT AUSTIN GPA: 3.8762
August 2019 – May 2021

Master of Science	Electrical and Computer Engineering
Relevant Coursework:	Power Electronics Modern Topics, Fundamentals of Power Electronics, Power Semiconductor Devices, Power Management IC Design, Analog IC Design, Nanoscale Device Technology

COLLEGE OF ENGINEERING PUNE, India GPA: 8.39
August 2015 – May 2019

Bachelor of Technology	Electrical Engineering
Relevant Coursework:	Power Electronics, Electric Drive, Electric Machinery, Power System Analysis, Solid State Devices and Linear Circuits, Engineering Mathematics, Control Systems

Research Experience

Low Leakage, Low Loss, High Frequency Energy-Storage Transformer August 2020 – May 2021

Supervisor:	Prof. Alex Hanson
Institute:	The University of Texas at Austin
Position:	Graduate Research Assistant
Funding:	Enphase Energy
Tools used:	Ansys Maxwell, LTSpice, MATLAB scripting
Related publications:	[1]

- The developed transformer used field shaping to achieve current conduction along most of the skin of the conductors, equal current sharing between the paralleled turns, even for out of phase currents, and near zero MMF drop across the leakage reluctance paths
- The transformer, thus, has low leakage inductance and low conduction losses without the use of litz wire and can be used effectively for multi-MHz operation
- Work involved simulation and optimization of the design in Ansys Maxwell as well as modeling and simulating the magnetic system in electrical domain using LTSpice to determine the optimum design parameters for the quasi-distributed air gaps and transformer core
- Step-by-step design guidelines were developed and a prototype transformer was built which achieved a leakage-to-magnetizing ratio of 1.12%, just 1/7th power loss of a conventional transformer, and almost equal current sharing between paralleled transformer turns

Pulsed Power Supplies for Electric Discharge Machining May 2018 – August 2018

Supervisor:	Prof. S. V. Kulkarni
Institute:	Indian Institute of Technology, Bombay
Funding:	Indian National Academy of Engineering (one of fifty students across India) National Center for Photovoltaic Research and Education
Tools used:	MATLAB Simulink, TINA-TI, Code Composer Studio, DSP (TMS320x2806x)
Related publications:	[2]

- Developed simulations for LCC resonant converter, 4-phase interleaved buck converter with coupled inductor based energy recovery, and thirteen other power supply topologies for delivering pulse power to machining load
- Identified trade-offs between each topology and developed efficiency calculation methodology for an EDM application
- A Tastekin converter was implemented and tested for a Wire-EDM machine for cutting silicon ingots
- Our work culminated in a Review Article published in IET Power Electronics Journal

SWAYAM Satellite and CSAT-2 January 2016 – May 2019

Supervisor:	Prof. Manisha Khaladkar	
Institute:	College of Engineering Pune	
Position:	Project Manager	Apr’18 - May’19
	Power Lead	Apr’18 - May’19
	Power Sub-system member	Jan’16 - Apr’18
Funding:	Indian Space Research Organization (ISRO)	
Related publications:	[3]-[8]	

- COEP’s Satellite Initiative (link) is a student satellite team of 40+ undergraduate researchers forming six subsystems - one of them being the Power Subsystem (of which I was first a member and later led the entire team as the project manager)
- SWAYAM project was aimed at developing a reliable bi-directional communications platform in the HAM frequency band enabling it to receive, store and transmit message from one corner of the globe to the other. It housed India’s first Passive Attitude Control system enabling it to stabilize and orient itself without consuming electrical power. SWAYAM, launched in 2016 by ISRO, was a full success.
- CSAT-2, a successor of SWAYAM, has a scientific objective of demonstrating orbit maneuvering using solar sails - another passive means of attitude and altitude control. The satellite will also house a payload to characterize charged particle environment in the Low Earth Orbit.
- My Contributions:
  * Implementation of Boost and Inverted Buck-Boost converters
  * Implementation of a 3-phase BLDC motor driver
  * Design of analog PID controller to control current draw of a BLDC motor as per the torque requirements
  * Design of a Load Protection system for various power system loads
  * In-orbit performance characterization of SWAYAM
  * Post launch testing and debugging on SWAYAM’s *Qualification Models*

Capacitive wireless power transfer - Simulations and feasibility study January 2020 – May 2020

Supervisor:	Prof. Alex Hanson
Institute:	The University of Texas at Austin

- Project aimed at determining feasibility for a loosely coupled, capacitive wireless power transfer based connector for applications in lunar/martian environments.
- Assisted with literature review, modeling and simulations and putting together proposals for the research project.

Publications

1. Nguyen, A., Phanse, A., Solomentsev, M., & Hanson, A. J. (2022, September). A low-leakage, low-loss magnetic transformer structure for high-frequency applications. In 2022 24th European Conference on Power Electronics and Applications (EPE’22 ECCE Europe) (pp. 1-11). IEEE. (link)
2. Kane, M. M., Phanse, A. A., Bahirat, H. J., & Kulkarni, S. V. (2020). Classification and comparative study of EDM pulse generators. IET Power Electronics, 13(14), 2943-2959. (link)
3. Phanse, A., Karaguppi, A., Murkewar, O., Thorat, S., Nalawade, M., Bhakare, O., & Gupta, A. (2019, July). Design, implementation and comparison of power electronic circuits for current control through 3-axis magnetorquer coils in a satellite. In 2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS) (pp. 1-6). IEEE. (link)
4. Waghulde, D., Kapgate, N., Pisal, S., Papal, S., Gajare, T., Rathod, B., ... & Phanse, A. (2016, November). Simulation, design and implementation of various MPPT systems for micro cube-satellite application. In 2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH) (pp. 80-84). IEEE. (link)
5. Design of a robust electrical power system of a 3u cubesat. Presented at 67th International Astronautical Congress.
6. Design and comparative analysis of novel technologies for reaction wheel torque control in accordance with attitude control law of satellite. Presented at 70th International Astronautical Congress.
7. Design and implementation of a resilient load protection system of a nano satellite. Presented at 68th International Astronautical Congress.
8. A potent and enduring electrical power system for a nanosatellite. Presented at 68th International Astronautical Congress.

Teaching Experience

Physics Lab - Electricity, Magnetism, and Optics Jan 2020 – May 2020

- Graduate Teaching Assistant for undergraduate Physics Lab
- Pre-lab lectures, lab demonstrations, evaluation and office hours

Industry Experience

Apple Inc. June 2021 – July 2024

Team:	iPhone Touch Hardware	
Position:	Hardware Development Engineer 3	Oct'22 - July'24
	Hardware Development Engineer 2	June'21 - Sept'22

- Part of iPhone Touch Electrical Engineering team responsible for the implementation of the Touch ASIC, its integration with the system, implementation of noise removal algorithms, and the design and modeling of the capacitive touch screen
- Design of flexible printed circuits to integrate the ASIC with the sensor panel and system SOC. Ensuring and determining design rules for mass production of hundreds of millions of these flexible printed circuits for iPhones
- Reliability testing of Touch sensing modules against environmental stresses to tease out failure modes and implementing correction actions for the same
- Developing infrastructure for post-processing sensor's raw data to visualize effects of system noise sources, thus aiding in failure analysis and debugging

Texas Instruments Inc. May 2020 – August 2020

Team:	Battery Charger Products
Position:	Analog Design Intern

- Worked on implementing a very low current consumption (<400nA) clock generating circuit
- Implemented two different architectures - Current Starved Ring Oscillator and Relaxation Oscillator
- Performed Monte Carlo simulations to ensure performance across PVT corners. Reliability simulations to ensure robust design.
- Implemented trimming strategies to compensate for process variation
- Design innovations led to circuit needing only 30% of allocated Si area and reduced post-fabrication test time

Academic Projects at UT-Austin

Design and optimization of an on-chip Buck converter with peak current control

- 1V output, 2.7-4.5V input with max load of 2A
- Included transistor level design of an error amplifier, gate driver, current sensor, comparator, deadtime generator, PWM logic, bandgap reference, and clock generator
- Part of PMIC coursework. Team of two.

Implementation of three DC-DC converters using the same canonical switching cell for undergrad demo

- Hardware implementation of a Buck, Boost and Buck-Boost converter
- On-board efficiency calculation displayed using a 7-segment display, CCM and DCM operation demo, implemented both synchronous and asynchronous modes of operation, demonstrated effects of ringing using variable loop inductance
- Part of "Power Electronics Modern Topics" coursework. Team of three.

Soft-switched Buck converter with Voltage Mode Control

- 12V output, 48V input, 60W converter with power density of $50W/in^3$
- Implements dead-time control and valley switching to achieve soft-switching
- Part of "Fundamentals of Power Electronics" coursework. Team of two.

Design of a 11.43-bit 50Msps, two-stage SAR based pipeline ADC

- 2-stage 50 mega samples per sec SAR sub-ADC based pipeline architecture with 5-bit first stage and 7-bit second stage
- Used a half-gain MDAC with a triple cascode telescopic amplifier. Implemented a dynamic comparator to achieve fast transient response. Used bootstrapped switches at the input sample and hold.
- SNDR: 70.53dB, SFDR: 80.5dB, ENOB: 11.43 bit at nyquist rate, Energy consumption: 52fJ/conversion step
- Part of "Analog-Digital Data Converters" coursework. Team of two.

Design of a two-stage fully differential Operational Transconductance Amplifier

- Telescopic cascode amplifier as first stage and PMOS-input differential amplifier as second stage
- Implemented common mode feedback
- Included transient simulations, noise analysis, and stability analysis
- Part of "Analog IC Design" coursework

Selected Academic Projects at COEP

Robust controller design for a quadcopter drone

- Implemented Sliding Mode Controller, Robust PID controller and Traditional PID controller for wind rejection. Validation and comparison done on a Pixhawk-4 embedded controller.
- Senior Design Project

3-phase inverter

- IGBT based inverter with sinusoidal PWM provided by a DSP

Honors and Awards

- Cockrell School of Engineering **Fellowship** — 2024 - 2028 (Expected)
- Summer Research **Fellowship**, Indian National Academy of Engineering (INAE) — 2018

Technical Skills

Skills	:	Power converters, Control Systems, Power Magnetics, Power Semiconductor Devices, Analog ICs
Simulation	:	Cadence Virtuoso, LTSpice, MATLAB Simulink, Ansys Maxwell
PCB Design	:	Allegro, Eagle, KiCad
Microcontrollers	:	Code Composer Studio
Documentation	:	Latex
Languages	:	Python, MATLAB Scripting/App Designer, C